CLAIMS

1. An electronic device, comprising:

an electronic component; and

an integrated circuit configured to generate a system clock and an external clock having a programmable delay from the system clock, the integrated circuit being further configured to provide the external clock to the electronic component to support communications therewith, communicate with the electronic component, and calibrate the external clock delay as a function of the communications.

2. The electronic device of claim 1 wherein the communications comprise a plurality of transmissions from the integrated circuit to the electronic component, the integrated circuit being further configured to program a different external clock delay for each of the transmissions, and calibrate the external clock delay as a function of the transmissions.

3. The electronic device of claim 1 wherein the electronic component comprises memory.

4. The electronic device of claim 3 wherein the integrated circuit is further configured to generate a feedback clock having a programmable delay from the system clock, the integrated circuit being further configured to use the external clock to write to and read from the memory, and use the feedback clock to sample data read from the memory.

5. The electronic device of claim 4 wherein the integrated circuit is further configured to calibrate the feedback clock delay as a function of the communications.

6. The electronic device of claim 5 wherein the communications comprise a plurality of read/write operations, the integrated circuit being further configured to program a different external clock delay and a different feedback clock delay for each of

the read/write operations, and calibrate the external clock delay and the feedback clock delay as a function of the read/write operations.

7. The electronic device of claim 6 wherein the integrated circuit is further configured to program the external clock delays and the feedback clock delays with a fixed offset between the external and feedback clocks for each of the read/write operations, and calibrate the external clock delay and the feedback clock delay with the fixed offset between the external and feedback clocks.

8. The electronic device of claim 7 wherein the integrated circuit is further configured calibrate the external clock delay and the feedback clock delay by determining the lowest delay between the system clock and one of the external and feedback clocks for a successful read/write operation and the highest delay between the system clock and said one of the external and feedback clock for a successful read/write operation, and selecting a delay therebetween, the selected delay being used to calibrate said one of the external and feedback clocks.

9. The electronic device of claim 8 wherein the selected delay comprises the center value between the lowest delay and the highest delay.

10. The electronic device of claim 3 wherein the memory comprises a Synchronous Dynamic Random Access Memory (SDRAM).

11. The electronic device of claim 1 wherein the electronic device comprises a wireless telephone.

12. A method of calibrating an integrated circuit to an electronic component, the integrated circuit having a system clock, comprising:

generating an external clock on the integrated circuit, the external clock having a programmable delay from the system clock;

providing the external clock from the integrated circuit to the electronic component to support communications therewith;

communicating between the integrated circuit and the electronic component; and

calibrating the external clock delay as a function of the communications.

13. The method of claim 12 wherein the communications comprise a plurality of transmissions from the integrated circuit to the electronic component, the method further comprising programming a different external clock delay for each of the transmissions, and wherein the calibration of the external clock delay is a function of the transmissions.

14. The method of claim 12 wherein the electronic component comprises memory.

15. The method of claim 14 further comprising generating a feedback clock on the integrated circuit, the feedback clock having a programmable delay from the system clock, and wherein the communications between the integrated circuit and the memory further comprise using the external clock to write to and read from the memory, and using the feedback clock to sample, at the integrated circuit, data read from the memory.

16. The method of claim 15 further comprising calibrating the feedback clock delay as a function of the communications.

17. The method of claim 16 wherein the communications between the integrated circuit and the memory comprise a plurality of read/write operations, the method further comprising programming a different external clock delay and a different feedback clock delay for each of the read/write operations, and wherein the calibration of the external clock delay and the feedback clock delay is a function of the read/write operations.

18. The method of claim 17 wherein the external clock delays and the feedback clock delays are programmed with a fixed offset therebetween for each of the

read/write operations, and wherein the external clock delay and the feedback clock delay is calibrated with the fixed offset therebetween.

19. The method of claim 18 wherein the calibration of the external clock delay and the feedback clock delay further comprises determining the lowest delay between the system clock and one of the external and feedback clocks for a successful read/write operation and the highest delay between the system clock and said one of the external and feedback clock for a successful read/write operation, and selecting a delay therebetween, the selected delay being used to calibrate said one of the external and feedback clocks.

20. The method of claim 19 wherein the selected delay comprises the center value between the lowest delay and the highest delay.

21. The method of claim 14 wherein the memory comprises a Synchronous Dynamic Random Access Memory (SDRAM).

22. The method of claim 12 wherein the integrated circuit and the electronic component form at least part of a wireless telephone.

23. An electronic device, comprising:

an electronic component; and

an integrated circuit including,

means for generating a system clock,

means for generating an external clock having a programmable delay from the system clock,

means for providing the external clock to the electronic component to support communications therewith,

means for communicating between the integrated circuit and the electronic component, and

means for calibrating the external clock delay as a function of the communications.

24. The electronic device of claim 23 wherein the electronic component comprises memory, and wherein the integrated circuit further comprises means for generating a feedback clock on the integrated circuit, the feedback clock having a programmable delay from the system clock, wherein the means for communicating between the integrated circuit and the memory is performed by using the external clock to write to and read from the memory, and using the feedback clock to sample data read from the memory, and wherein the integrated circuit further comprises means for calibrating the feedback clock delay as a function of the communications.

25. Computer readable media embodying a program of instructions executable by a processor to perform a method of calibrating an integrated circuit to an electronic component, the integrated circuit including a system clock and an external clock having a programmable delay from the system clock, the external clock being provided to the electronic component to support communications therewith, the method comprising:

communicating between the integrated circuit and the electronic component; and

calibrating the external clock delay as a function of the communications.

26. The computer readable media of claim 25 wherein the electronic component comprises memory, and wherein the integrated circuit further includes a feedback clock having a programmable delay from the system clock, wherein the communication between the integrated circuit and the memory is performed by using the external clock to write to and read from the memory, and using the feedback clock to sample data, at the integrated circuit, read from the memory, and the method further comprises calibrating the feedback clock delay as a function of the communications.